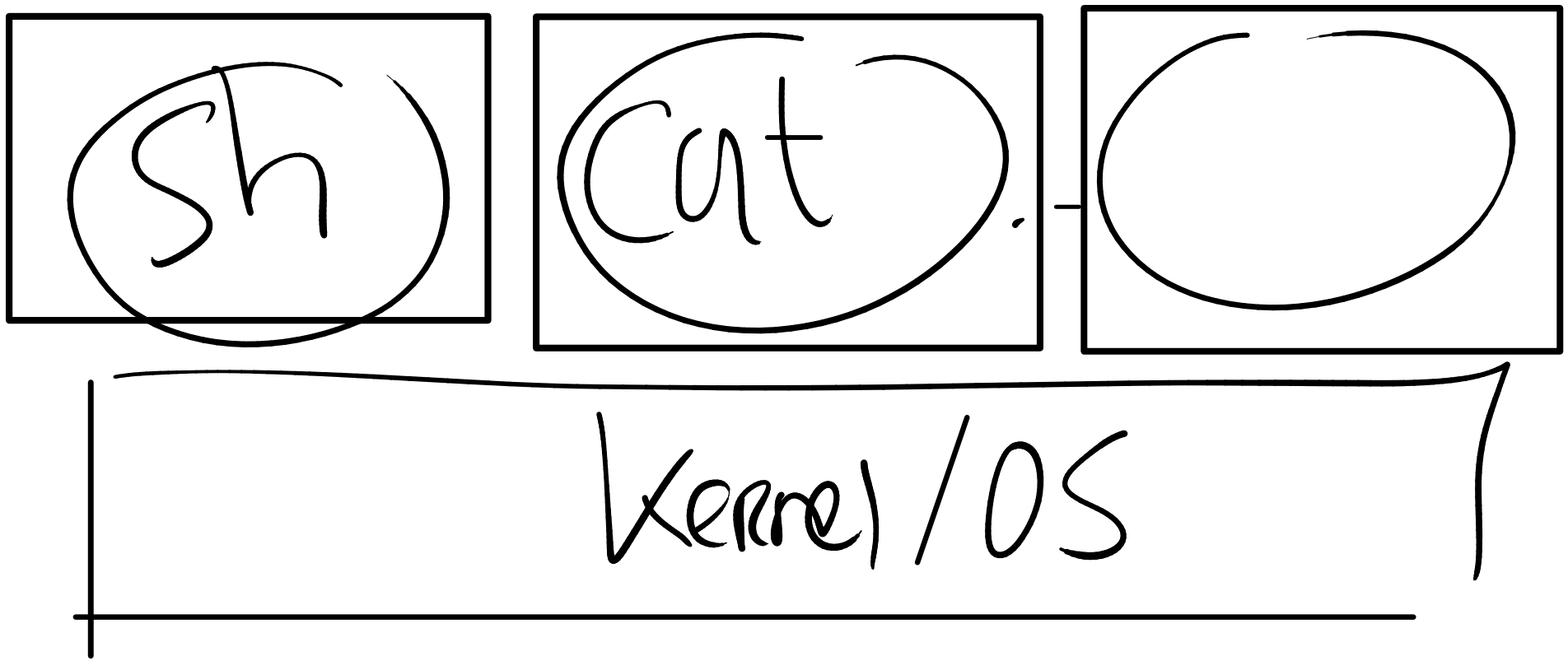
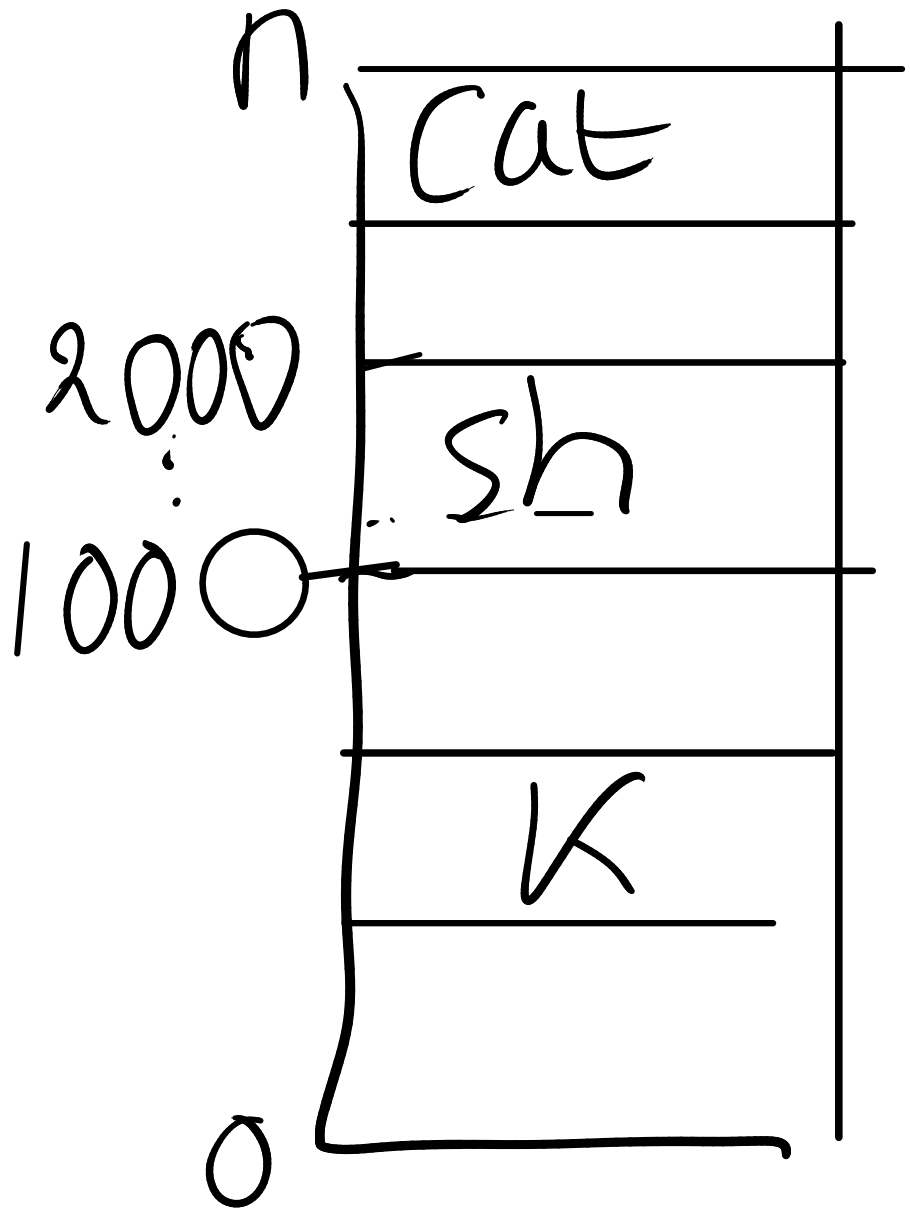
6.S081 : page tables (VM)

plan:
1) Address spaces
2) paging hw (RISC-V)
3) xv6 vm code + layout

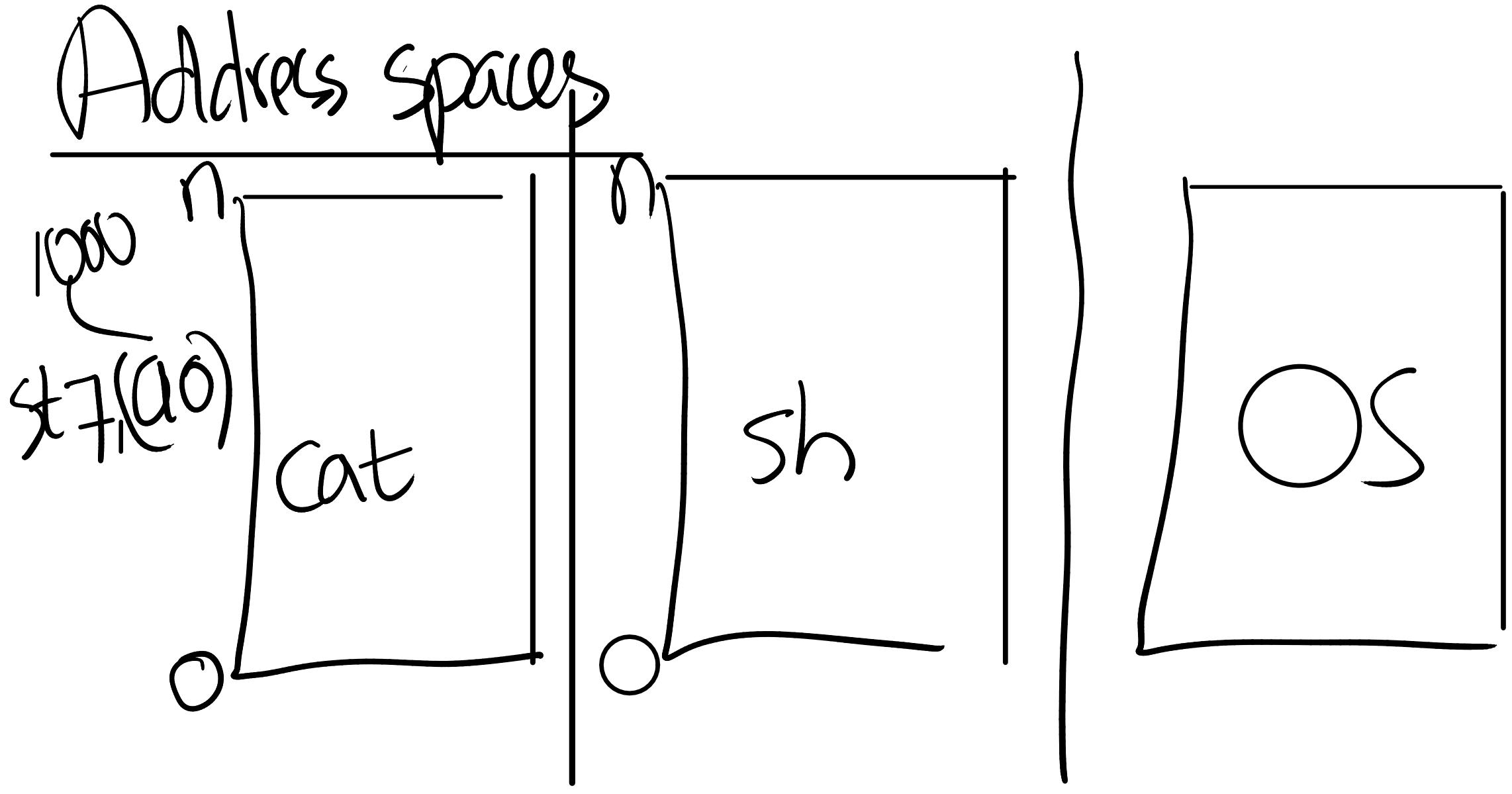
Isolation



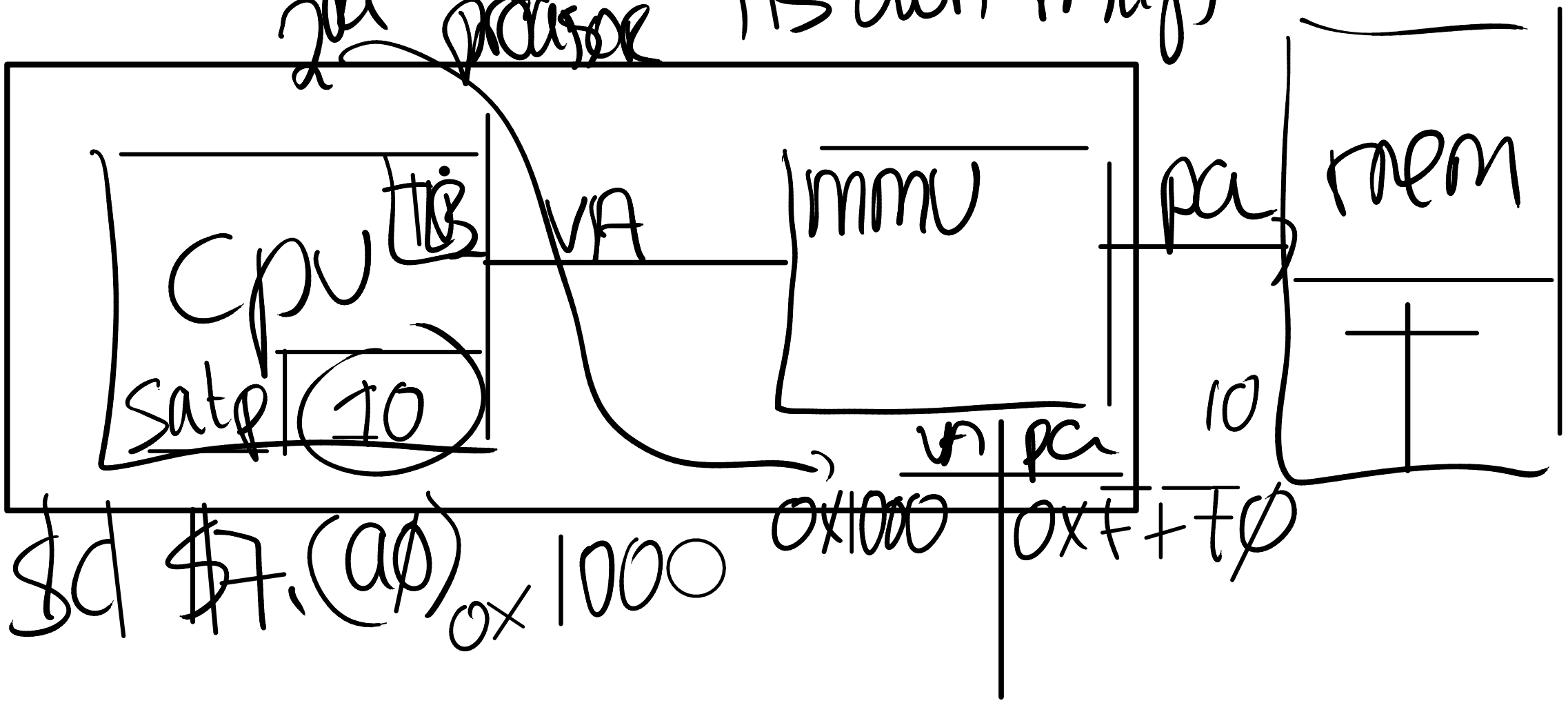
Memory




```
ldaφ, 1000
sd $7, (aφ)
```


Address spaces
n
1000
st 7,(a0)
cat
n
sh
OS

pagetables (tw) every app has its own map

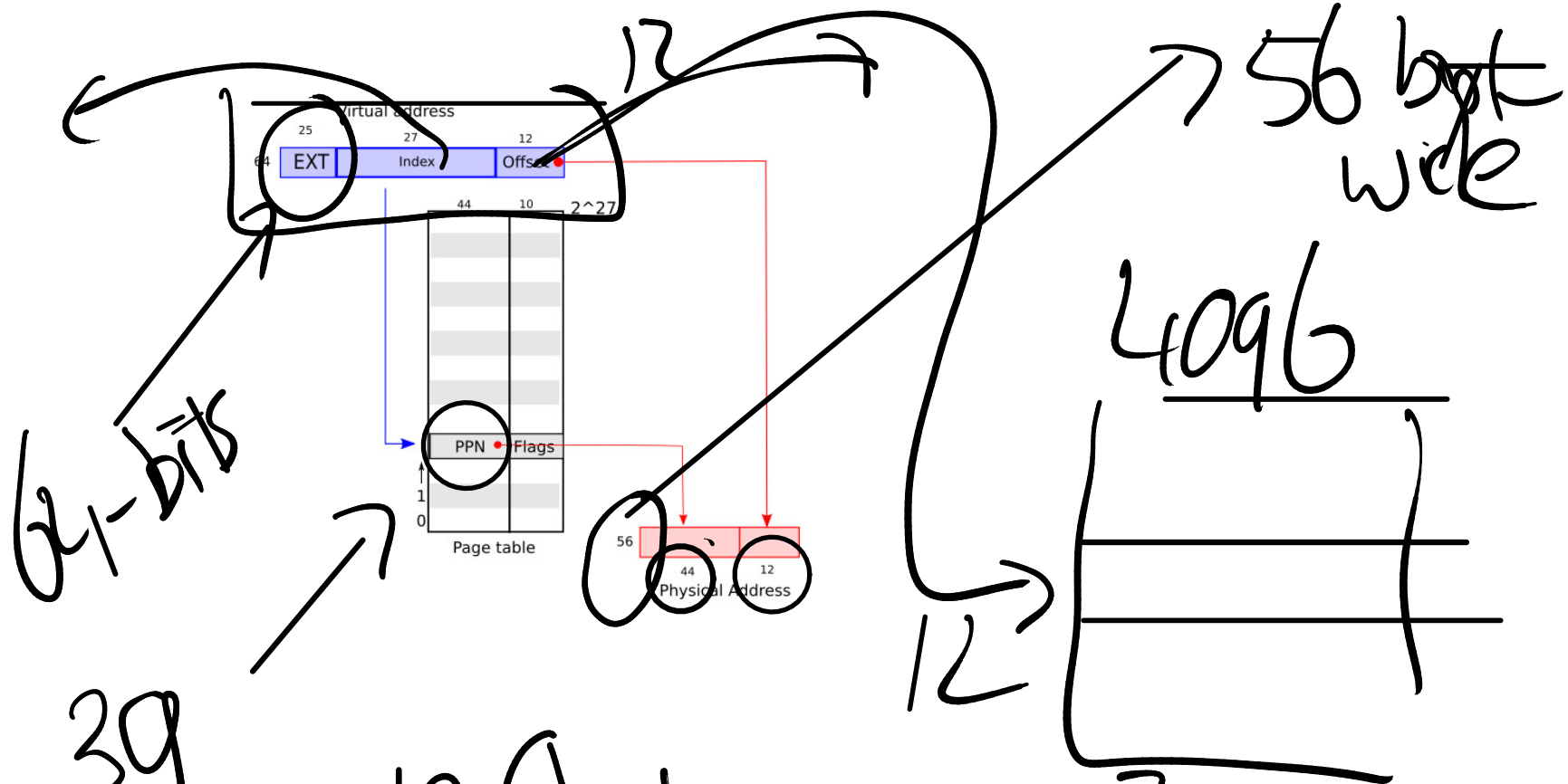


Per page

4 KB

4096

2^{27}



64-bits

12

56 bit wide

4096

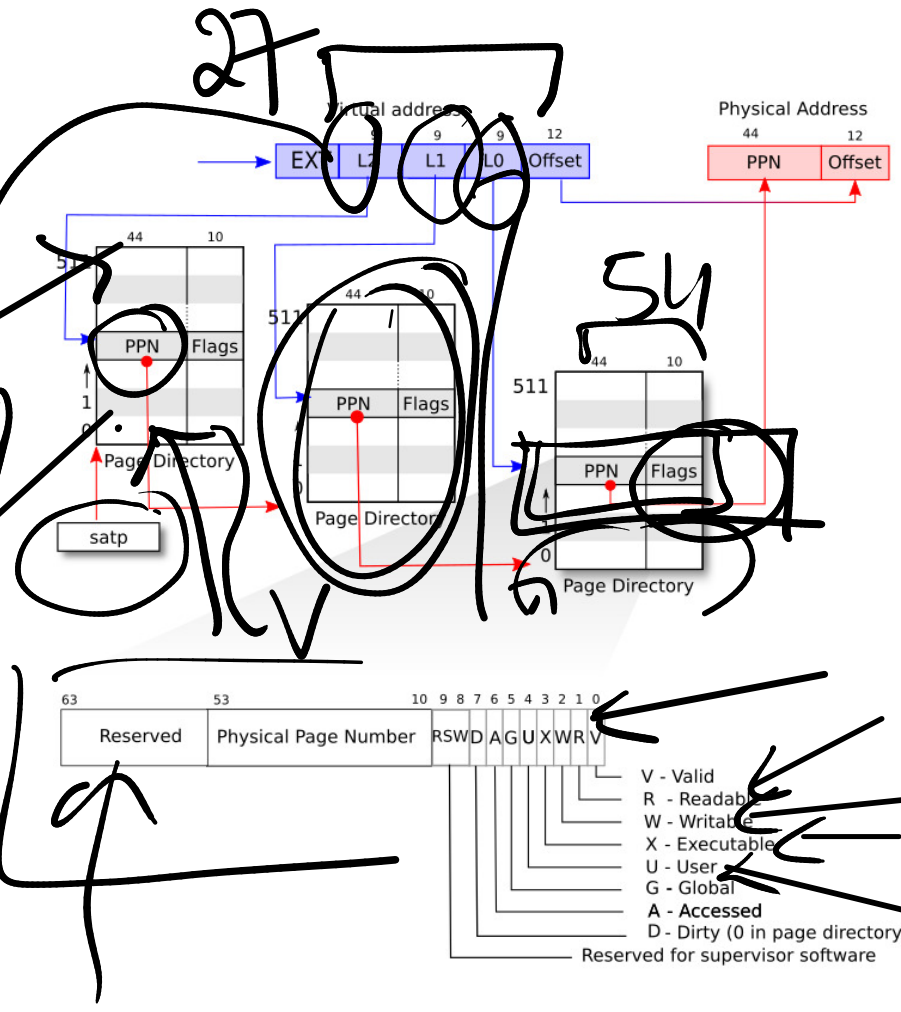
$2^{39} \approx 512$ Gbyte

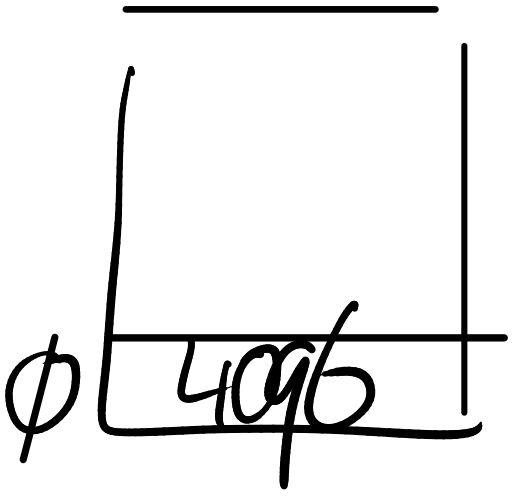
27 bits are index,

$2^{12} = 4096$

12 offset

RISC-V page table





4096

64 bits (8)

4096/8 = 512

44+12=56

3 page directory

Translation look-aside buffer (TLB)

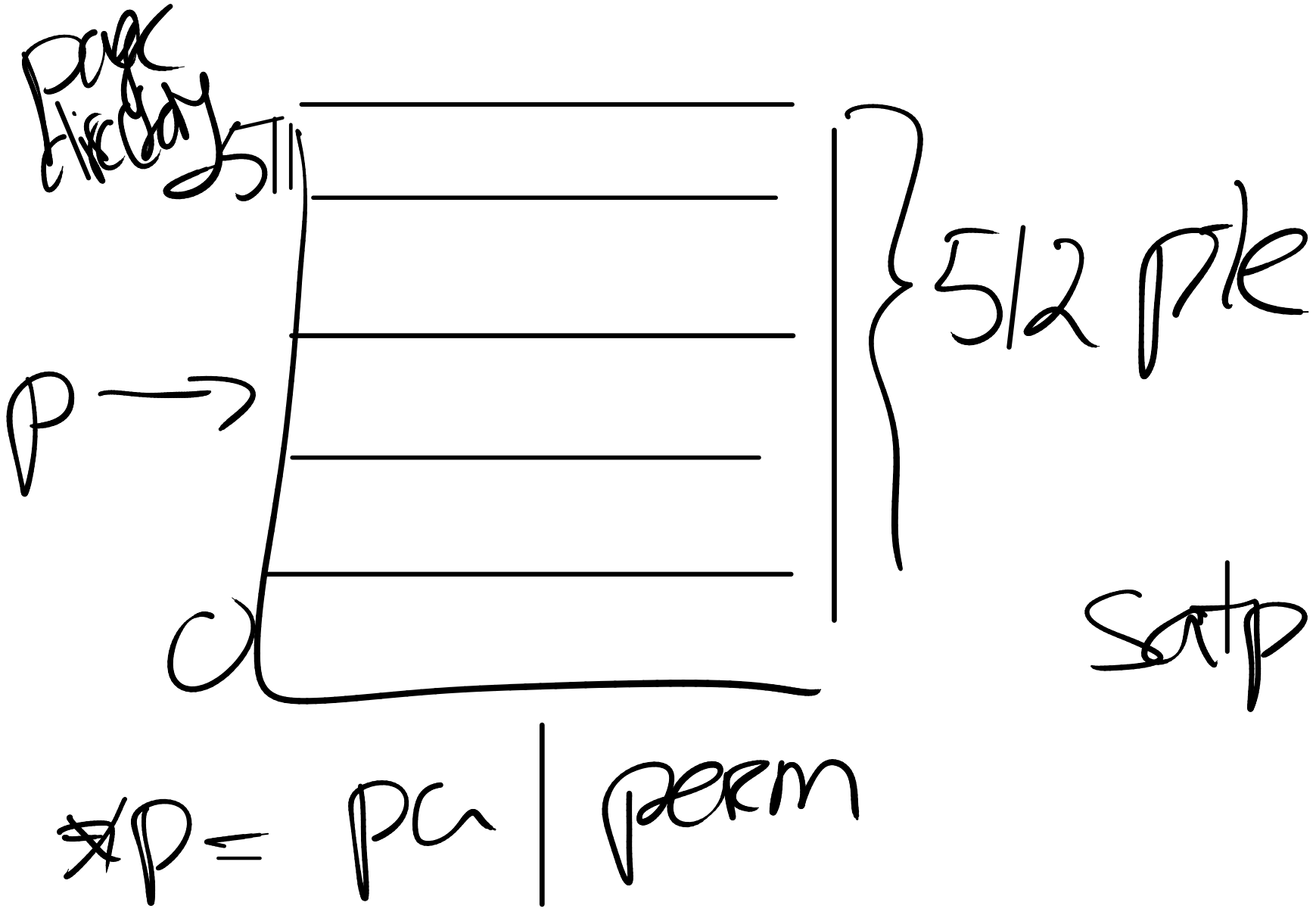
Cache of pte entries

[VA, PA] space_vma

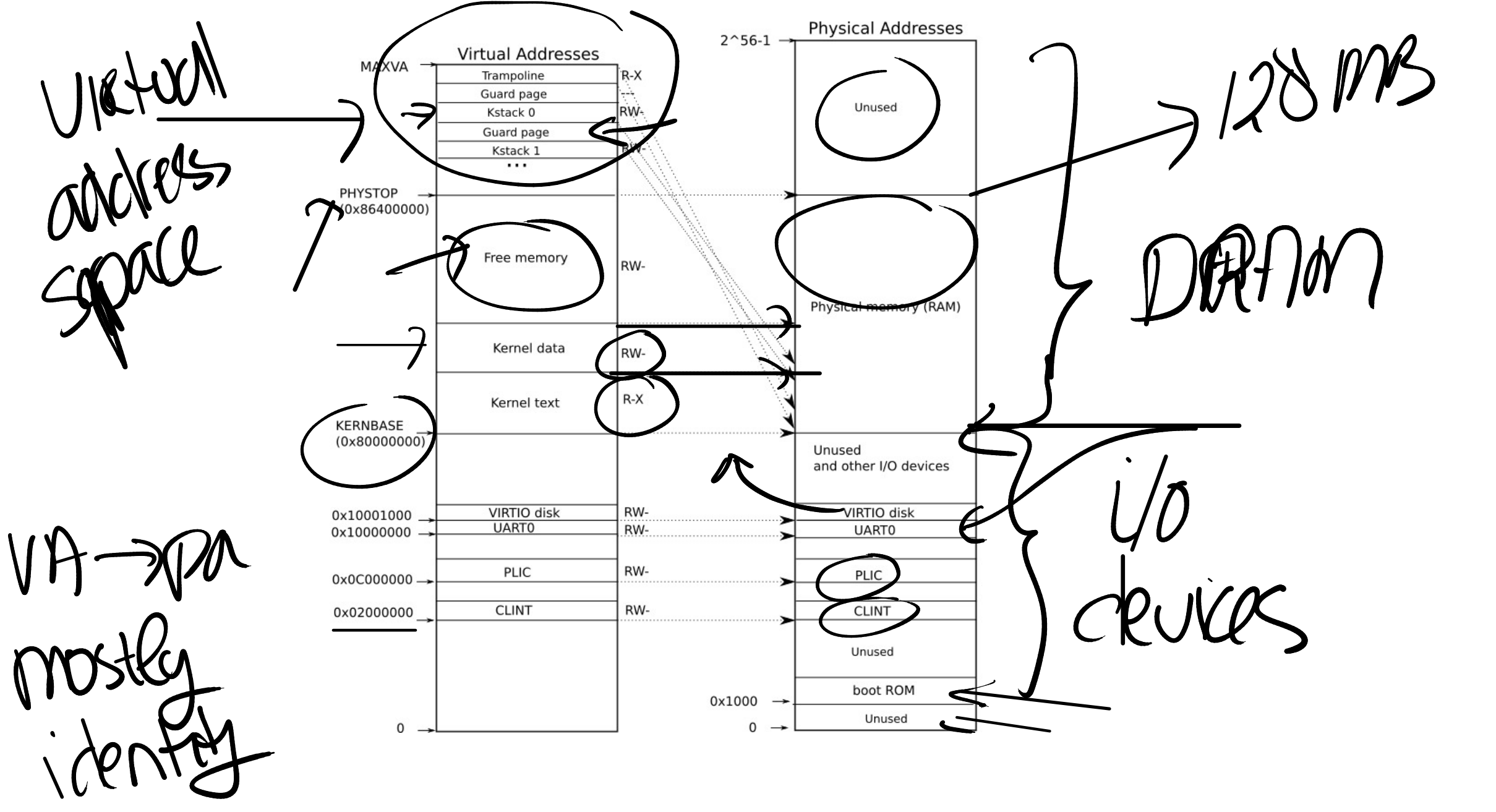
Switch page table ⟹ flush TLB

Page tables source level of interaction

under control of OS



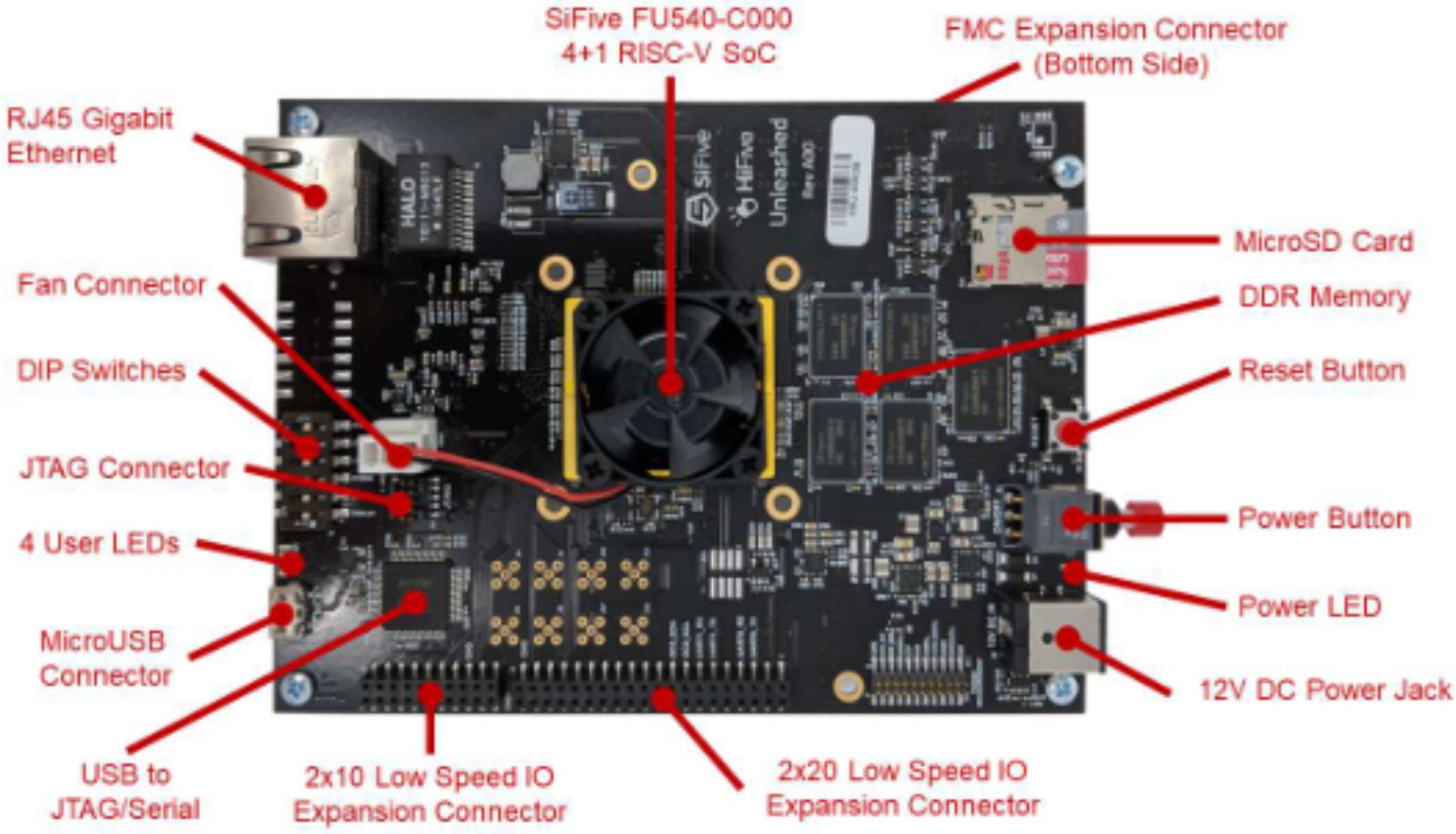
*p = pa | perm

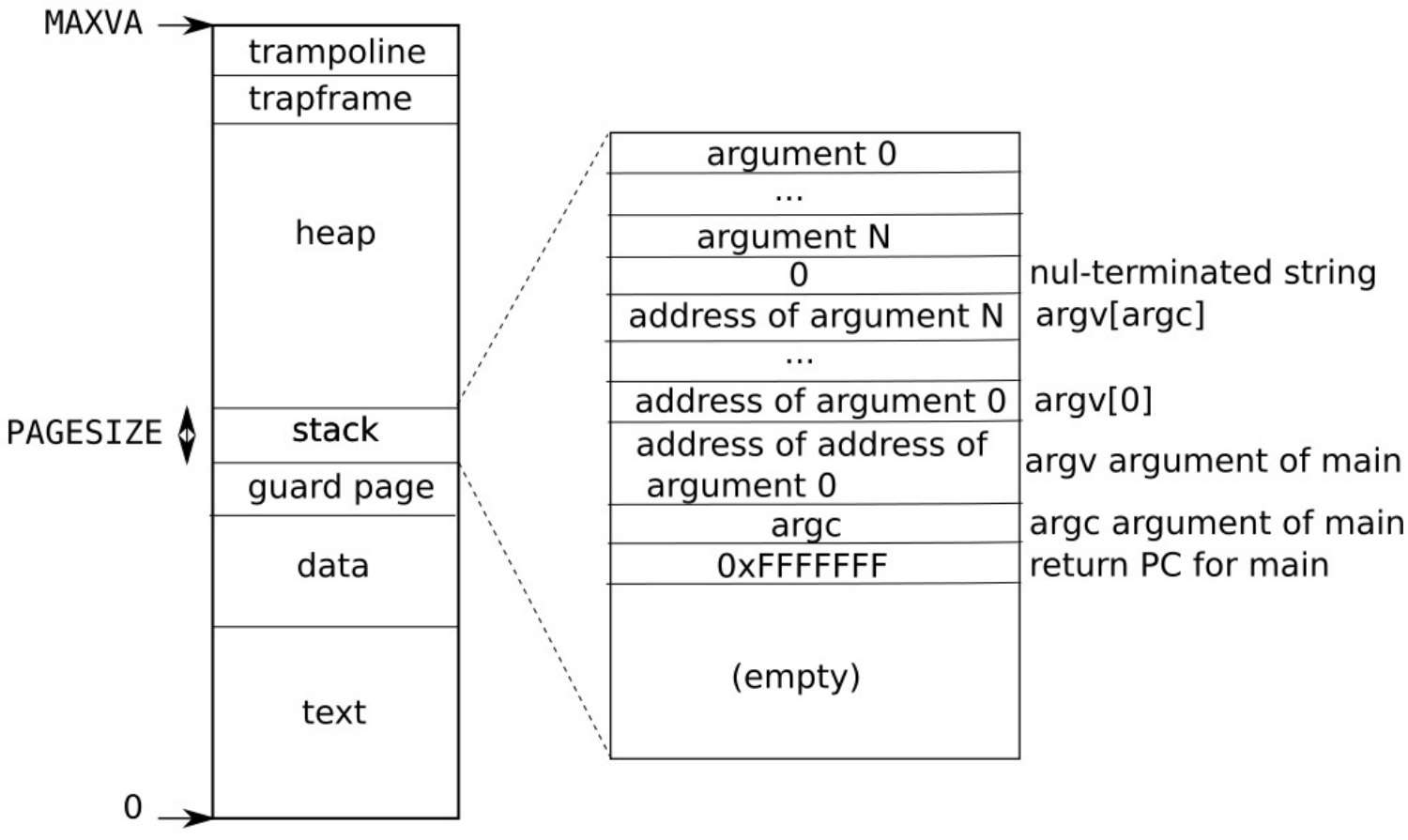

Virtual Addresses
MAXVA
Trampoline
R-X
Guard page

Kstack 0
RW-
Guard page

Kstack 1
RW-
PHYSTOP
(0x86400000)
Free memory
RW-
Kernel data
RW-
Kernel text
R-X
KERNBASE
(0x80000000)
0x10001000
VIRTIO disk
RW-
0x10000000
UART0
RW-
0x0C000000
PLIC
RW-
0x02000000
CLINT
RW-
0
Physical Addresses
2^56-1
Unused
Physical memory (RAM)
Unused
and other I/O devices
VIRTIO disk
UART0
PLIC
CLINT
Unused
0x1000
boot ROM
Unused
0
Virtual address space
128 MB
DRAM
I/O devices
VA → PA
mostly identity


HALO
SiFive
0x8000


SiFive FU540-C000
4+1 RISC-V SoC
FMC Expansion Connector
(Bottom Side)
RJ45 Gigabit
Ethernet
MicroSD Card
Fan Connector
DDR Memory
DIP Switches
Reset Button
JTAG Connector
Power Button
4 User LEDs
Power LED
MicroUSB
Connector
12V DC Power Jack
USB to
JTAG/Serial
2x10 Low Speed IO
Expansion Connector
2x20 Low Speed IO
Expansion Connector


MAXVA
trampoline
trapframe
heap
PAGESIZE
stack
guard page
data
text
0
argument 0
...
argument N
0
address of argument N
...
address of argument 0
address of address of argument 0
argc
0xFFFFFFF
(empty)
nul-terminated string
argv[argc]
argv[0]
argv argument of main
argc argument of main
return PC for main