

The Low-Cost Packet Radio

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Invited Paper

Research on packet switched radio networks requires reconfigurable testbeds with large numbers of readily deployable radios. This motivated the development of a small, low-cost packet radio (LPR) with the flexibility to support extensive network experiments, and to be amenable to tailoring to specific end-use applications.

The LPR incorporates a digitally controlled direct sequence minimum shift keyed spread-spectrum radio and a microprocessor-based packet switch. Code changeable surface acoustic wave (SAW) matched filtering provides processing gain at burst symbol rates of 100k and 400k symbols per second in the presence of interference. Coherent recursive integration enhances synchronization performance, provides synchronous detection of the data, and serves the adaptive multipath accumulator. Forward error correction utilizing convolutional encoding and sequential decoding is incorporated at four different code rates for both burst symbol rates. The microprocessor runs the networking software.

Requirements, design, and performance data for the LPR engineering model are presented.

I. INTRODUCTION

The Low-Cost Packet Radio (LPR) is the current generation packet radio supporting the development and evaluation of advanced packet networking concepts, techniques, and protocols. The LPR comprises radio frequency (RF) transmission and reception capabilities, and a programmable digital processor which together provide the functionality of the lower three levels of the International Standards Organization (ISO) Open System Interconnection Reference Model; viz, the Physical, Link, and Network Layers.

This paper describes the hardware implementation of the LPR; the component of a packet network between the wire interface and the RF interface. As an introduction to packet radio in general, Section II defines its functions and addresses some major issues. Section III presents the more important functional requirements and specifications

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placed on the LPR that are necessary to support the large testbeds planned for the development of advanced packet switching networks. Section IV describes the hardware design. The emphasis is on those features needed to provide the functionality and performance essential to the LPR. The expected performance is compared to measured performance on several development models in Section V, followed by conclusions in Section VI.

II. PACKET RADIO FUNCTIONALITY CONSIDERATIONS

This section describes the hardware functionality requirements of a packet switching node in the DARPA Packet Radio Network [1], the chief obstacles to obtaining the desired functionality, and techniques for overcoming these obstacles.

A. Radio Functionality

To operate as a node in the DARPA packet radio network, a packet radio requires a processor section to control the routing and flow between packet radios, and a radio section to transmit and receive packets over the channel. Capability to provide many different operational settings of the radio to better match the radio to the large variations expected to be encountered in the channel characteristics is desirable. The radio may vary the following parameters:

- Forward Error Correction (FEC) Capability
- Multipath Accumulation Interval
- Data Rate
- Symbol Rate
- Transmitted Power.

To set the radio properly, metrics necessary to estimate the channel characteristics are required.

In addition to an interface with the radio section, the processor also requires a wire interface to connect a collection of devices (host computer, terminals, network monitor/controller, etc.) that may be connected to the packet radio. An interface to the processor to allow local debugging and program loading is also needed.

Ideally, the performance of the packet radio network would be bounded only by the channel capacity. Additionally, any necessary algorithmic computations and data

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processing should minimally impact network performance.

To fulfill the radio section requirements, the receiver must acquire, track, and demodulate the entire packet successfully. To acquire a packet, its presence must first be established and the occurrence of the critical packet events synchronized. The critical events are bit synchronization, frame synchronization, and, if coherent demodulation is used, phase synchronization [2], [3]. For communications efficiency, it is desirable that the time to acquire be short compared to the total packet length.

The acquisition of a packet is probabilistic, and depends on two factors:

- 1) the number of false alarms permitted,
- 2) the received signal-to-noise ratio (SNR).

Since a packet cannot be received if the receiver is processing a false alarm, the percentage of the time used in false alarm processing should be small. The probability that a packet is received with all bits correctly detected is a function of the bit error rate (BER), the number of bits in a packet, and the probability of acquiring the packet. The probability of acquisition and the probability of correctly demodulating the packet should be chosen to provide a robust and balanced capability for both processes.

B. Channel Characteristics

In general, the channel attenuates and distorts the signal and adds interference. The channel attenuation and distortion between any two randomly selected terrestrial points is a function of 1) the frequency, 2) the terrain profile, 3) the height of the two antennas above ground, and 4) the obstructions in the propagation path. As no two identical profiles exist, any prediction, statistical or otherwise, is an approximation at best. Hills, trees, buildings, and the atmosphere all act as scattering objects, causing the received signal to consist of a linear combination of many paths. The unknown phase relationship between paths with small delay differential may cause destructive interference or reinforcement of the signal. Variations of these path lengths caused by movement of the scattering objects, movement of the communicating nodes, or atmospheric anomalies, will cause attenuation variation (fades) with time, and also frequency. In many packet radio situations these fades may occur within a packet duration. Experiments have shown that the variation in multipath delay may reach $6 \mu\text{s}$ in urban environments [4].

The desired transmission is also received in the presence of network self-interference, which, in turn, depends on the channel access technique, the density of the network, and the traffic load. Other forms of expected interference include receiver thermal noise, background man-made noise such as automobile ignition, rotating machinery, etc., and interference from other transmission systems.

Direct sequence spread-spectrum is a well-known technique for reducing the effects of multipath and interference [5], [6]. With direct sequence spread-spectrum signals, each individual symbol is replaced by many independent shorter chips. All multipaths that have differential path delays greater than the chip duration and less than the symbol duration are converted from components that cause fading into components that cause interchip interference. In ad-

dition, the spread-spectrum correlation processing function provides discrimination between the interfering components so that the signal from each resolvable path may be independently tracked, demodulated, and combined thereby maximizing data demodulation performance [5].

C. Channel Access Techniques

Gaining access to the radio channel is a critical function of the radio in a packet radio network. Two multiple access techniques are to be used to support the packet radio network experiments being carried out under the DARPA program.

The carrier sense multiple access (CSMA) technique attempts to eliminate self-interference caused by transmissions on other links by sensing the channel prior to transmission. However, interference may still occur because of the "hidden terminal problem" [7], [8]. A hidden terminal refers to a transmitting terminal that is not heard at a terminal that is about to transmit, but is heard at an intended receiving terminal where both transmissions arrive concurrently.

The code division multiple access (CDMA) technique permits concurrent transmissions. The radio's anti-jam margin (AJM) mitigates the effects of concurrent reception. Studies have shown the spread-spectrum processing gain (PG) needed to support M CDMA concurrent transmissions is about $M/0.3$ [9]. More recent studies show that in the presence of fading in urban and suburban environments substantially more processing gain to support M CDMA channels may be required [10].

These access techniques are to be studied in a testbed environment (as analytic and simulation approaches to date are not sufficient) to develop and evaluate packet radio network capability.

III. LPR FUNCTIONAL REQUIREMENTS AND SPECIFICATIONS

The requirements placed on the development of the LPR are oriented toward its intended use: a radio to support large testbeds for further research and development on radio-based store-and-forward packet switching networks. This section defines the more important functional and performance requirements of the LPR.

A. Functional Requirements

The LPR is functionally divided into two sections, the radio section and the microprocessor section. The radio section of the LPR is required to modulate and transmit, receive and demodulate, and transmit packets between the microprocessor and the RF domain. The primary performance goals for the LPR are specified for a line-of-sight communications range of 10 km in a rural environment with rolling hills 15–45 m high. The antenna is assumed to be 1.5 m above ground. Based on the use of the Longley-Rice propagation model [11], [12], the LPR shall achieve:

probability of correct packet detection	≥ 95 percent
probability of false packet detection	$\leq 10^{-6}$
undetected bit error rate	$\leq 10^{-12}$
bit error rate, 100-kbit/s uncoded mode,	$\leq 10^{-5}$.

To support these goals, the radio is specified to operate with the RF characteristics summarized in Table 1.

Table 1 RF Signal Characteristics

Transmit power	5 W
Band of operation	1718.4 to 1840 MHz
Number of channels	20
Channel separation	6.4 MHz
Channel bandwidth	20 MHz
Modulation type	pseudorandom noise, direct sequence spread spectrum (DSPN)
Chip modulation	minimum shift keying (MSK)
Bit modulation	coherent phase shift keying (PSK)
Chip rate	12.8 megachips per second (MCPS)
Preamble	28 bits

Previous packet radio development programs have demonstrated that these goals are achievable with margin for equivalent waveform characteristics and with 10 W of transmit power [7]. For the LPR development, a 5-W transmit power is used, trading link margin for reduced size, weight, and power consumption.

The LPR must be provided in a rugged package of less than 760 in³, weighing less than 25 lb, and consuming less than 110 W at 50-percent duty factor.

To provide for experimentation in advanced networking techniques and protocols, the LPR is required to provide flexibility, under control of protocols, for the following performance parameters:

- alternative multiple access techniques
 - carrier sense multiple access (CSMA)
 - code division multiple access (CDMA)
- convolutional encoding and sequential decoding for FEC with a choice of
 - variable rates: 1/2, 3/4, 7/8, uncoded
 - hard and soft decision (2-bit)
- variable symbol rates
 - 100k symbols per second (kSPS)
 - 400kSPS
- 24-dB output power control selectable in 8-dB steps.

To support either of the two transmit rates and one of the four FEC options, the LPR is required to operate in one of eight modes of operation. These modes, selectable by microprocessor control, are identified in Table 2.

Table 2 Selectable Modes of Operation

Mode	Transmit Rate (kSPS)	Transmit Rate (kbits/s)	Transmit Format	Transmit Code Rate
1A	100	100	CRC*	
1B	100	50	FEC	1/2
1C	100	75	FEC	3/4
1D	100	87.5	FEC	7/8
2A	400	400	CRC*	
2B	400	200	FEC	1/2
2C	400	300	FEC	3/4
2D	400	350	FEC	7/8

*One or two 32-bit Cyclic Redundancy Checksums (CRCs) per packet shall be selectable.

The required FEC convolutional encoder/sequential decoder has a code constraint length of 36 at code rate 1/2, 63 at rate 3/4, and 91 at rate 7/8. The specified fixed interleaving process is in 128-bit blocks.

The required transmitted signal is a DSPN spread-spectrum waveform with MSK chip modulation. The DSPN code is required to be derived from the National Bureau of Standards Data Encryption Standard (DES) at a 12.8-MCPS (mega-

chips per symbol) rate, and is changeable from symbol to symbol [13].

Selection of RF frequency is required to be under microprocessor control. Any one of 20 frequencies in the tuning range, nominally 1718 to 1840 MHz, may be selected at 6.4-MHz increments. A new selection may be made on each successive packet. The frequency source is required to be stable to within $\pm 1/2$ part per million (ppm).

The dynamic range is required to be at least 80 dB, with a maximum signal level of -20 dBm and an 8-dB maximum noise figure. Automatic Gain Control (AGC) is to be provided with short settling time (less than two symbols at the 100-kSPS rate).

The LPR is required to make the following measurements available to higher layer protocols to help these functions set the physical layer modes:

transmit/receive status
 FEC error count
 packet time of arrival
 received signal plus noise level
 noise level
 multipath presence
 AGC level.

The following physical layer parameters will be controllable:

On Transmit	On Receive
• packet sectioning	• frequency
• FEC coding rate	• table of qualifiers
• preamble content	• time slot duration
• time enable	• DSPN code key
• data rate	• symbol hard/soft decision
• DSPN code key	
• time slot duration qualifier	
• frequency	
• RF output level	

The microprocessor section is required to host the protocols, performed in software [1]. To support the processing of these protocols it has been determined that the microprocessor is required to achieve a speed of at least 0.2 million instructions per second (MIPS) and to provide 64K bytes of ROM and 96K bytes of RAM.

IV. LPR DESIGN DESCRIPTION

The LPR, nomenclatured the AN/PRC-118 (), is currently in limited production for experimental use. Fig. 1 shows the completed development model along with the size, weight, and power consumption that have been achieved. From the figure it is noted that the only operations required of the user, once the antenna is connected, are to turn the radio on/off and optionally to connect the users' equipment to the HDLC and RS-232 ports. The simple display shows the radio's operational status.

A. Overview of LPR Implementation

Packets containing header and data are input to the LPR processor via a) the wire connection to the HDLC port or b) the RF link and the LPR receiver (Fig. 2). The data portion of the packet may contain either data to be forwarded to a host or control information for use by the local processor.

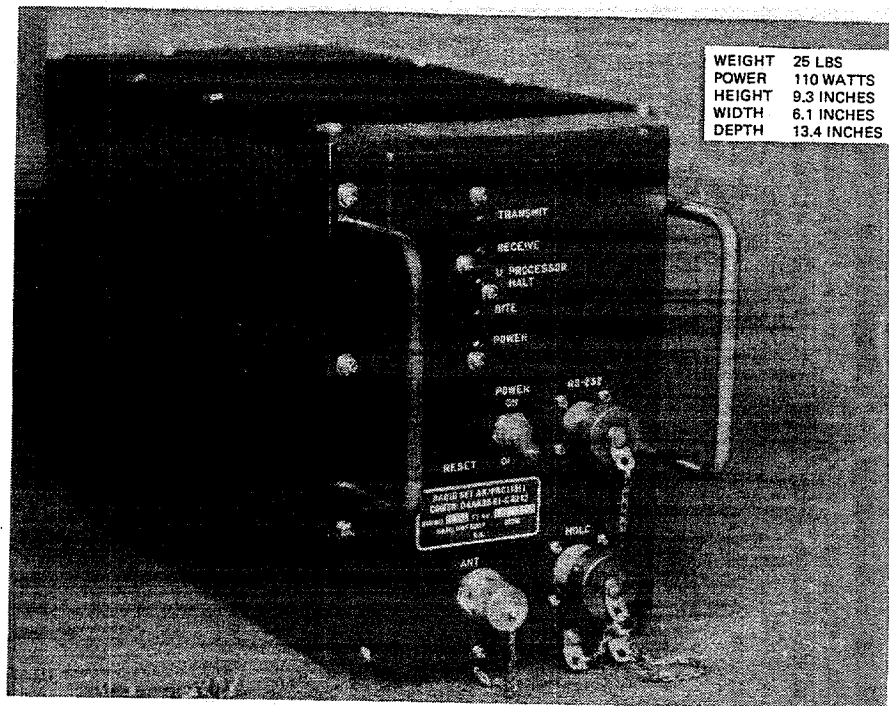


Fig. 1. The low-cost Packet Radio.

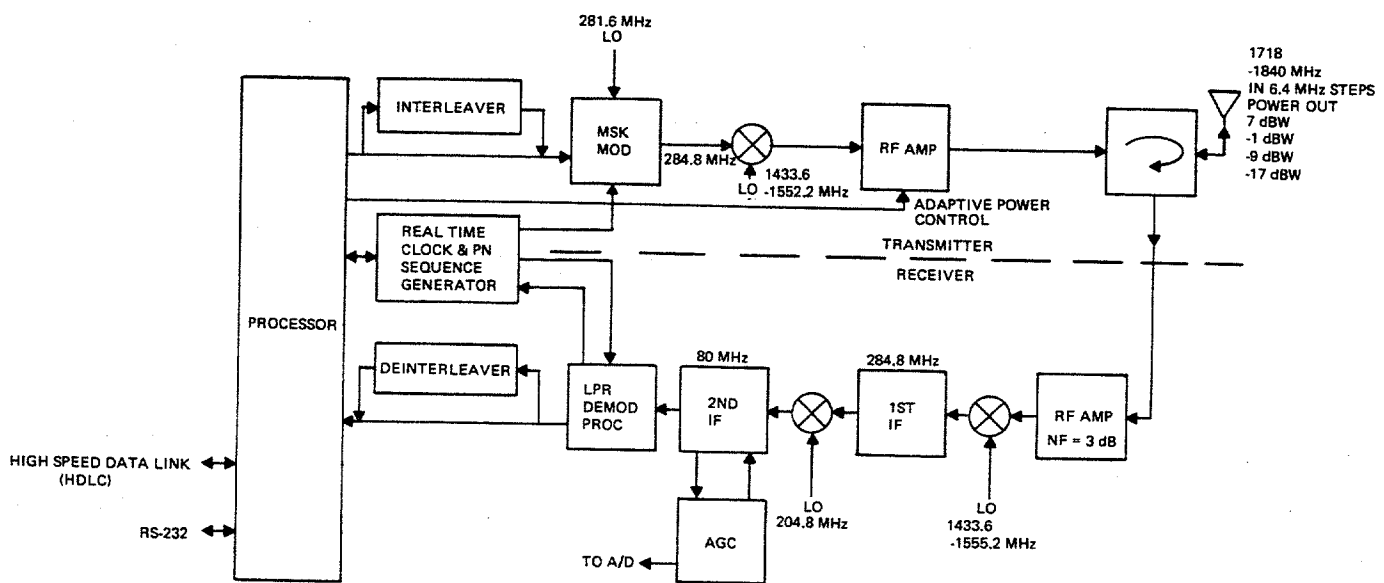


Fig. 2. LPR system basic block diagram.

The protocols resident in the LPR processor determine from the header and the state of the radio the proper disposition of the packet.

Referring to Fig. 2, CRC and FEC encoding of the data are done in the processor, interleaved (if in an FEC mode), and added modulo-2 to the DSPN spectrum spreading code. The 12.8-MCPS bit stream modulates a 281.6-MHz carrier supplied by the local oscillator (LO). The modulator implements the Amoroso technique [14] resulting in an MSK spread-spectrum signal at an intermediate frequency (IF) of 284.8 MHz, with PSK data modulation. This signal is up-converted to one of twenty selectable RF transmission frequencies. Upper layer protocols determine which frequency. The L-band signal is amplified and transmitted at one of four protocol selectable power levels.

On receive, the incoming signal is amplified in a low-noise amplifier, converted to the first IF of 284.8 MHz, amplified, converted to the second IF of 80 MHz, and amplified in the automatic gain controlled IF amplifier (bandwidth 12.8 MHz). The IF spread-spectrum output is demodulated via matched filtering and coherent processing and the data are passed to the receive processor.

B. Transmitter Signal Processing

The basic wide-band waveform used in the LPR is a direct sequence spread-spectrum signal utilizing MSK modulation with a chipping rate of 12.8 MCPS [2], [3], [14]. This yields a spreading factor (chips per symbol), of 32 for the 400-kSPS mode (2.5- μ s symbol), and a spreading factor of 128 for the 100-kSPS mode (10- μ s symbol). The spreading sequence

(obtained from the National Bureau of Standards DES algorithm) yields codes that are random with respect to each other and mitigates against the effects of self-jamming, incidental interference, intentional jamming, and multipath fading. The preamble uses a repetitive pseudonoise (PN) code sequence while the sequence for each data symbol varies from symbol to symbol to effect continuous code change. The symbol sequence and the PN sequence are synchronized with each other.

The modulo-2 combined PN spreading sequence and data symbol phase shift key the LO and the resultant signal is passed to the surface acoustic wave (SAW) filter in the MSK modulator [14], [15]. The MSK output signal is converted to one of 20 selectable L-band RF channels, amplified, and transmitted. The 5-W maximum transmitter has four selectable power levels controlled by the upper layer protocols, providing a power range of 24 dB in 8-dB steps. Both the power level and RF are selectable on a packet basis.

C. Receiver Signal Processing

The received signal, after downconversion, IF amplification, and AGC, is sent to the LPR demodulator processor shown in Fig. 3. In the demodulator the programmable matched filter (MF) strips off the PN spreading sequence, leaving a compressed pulse that is PSK modulated by the packet symbols (preamble, header, data, etc.).

1) *LPR Matched Filter*: A block diagram of the LPR programmable matched filter implementation is shown in Fig. 4. A chip filter matched to an individual MSK chip is followed by a tapped delay line with taps spaced at the chip duration (78.125 ns). The outputs of the taps are fed to either a plus or a minus bus according to the expected PN code, and the outputs of the two busses are subtracted to form the filter output. The matched filter is implemented using SAW techniques [15]. Fig. 5 shows a photograph of the LPR SAW matched filter. The chip filter is contained in the launching transducer and the tap outputs are fed to an integrated circuit which routes them to the plus and minus

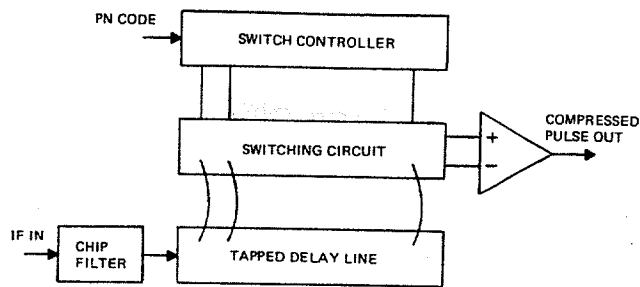


Fig. 4. Matched filter block diagram.

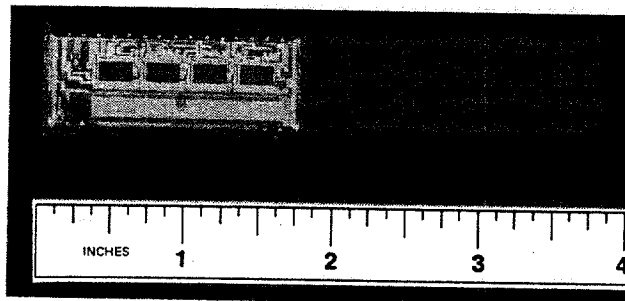


Fig. 5. LPR SAW matched filter.

bus according to the PN code. Each of the four integrated circuits sums 32 tap outputs. In the 128-tap mode (100-kSPS rate) the outputs of the integrated circuits are added together while in the 32-tap mode (400-kSPS rate), the output of only the first integrated circuit is used. The MF output is sent to the data demodulator and, after a one-symbol delay, to the decision directed coherent recursive integrator (CRI) [16].

2) *LPR Coherent Recursive Integrator*: The CRI provides enhanced carrier and multipath profile signals needed for coherent carrier demodulation in the data demodulator, and, after envelope detection, for use in determining signal acquisition. The performance of these functions is im-

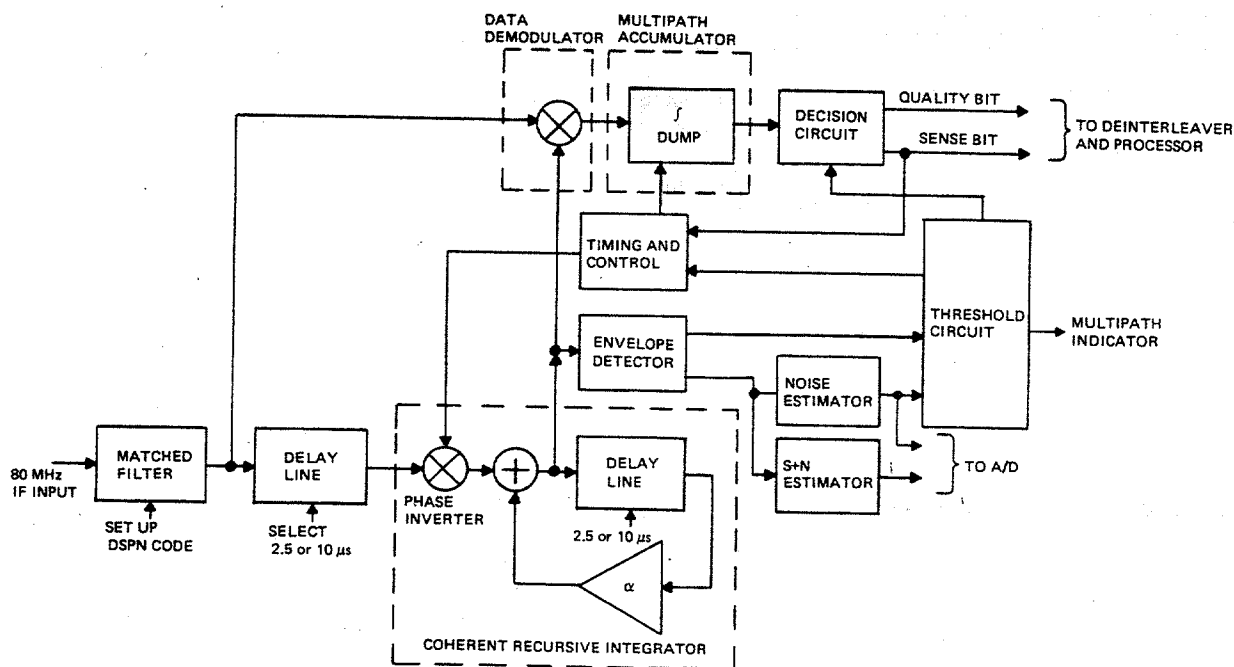


Fig. 3. LPR demodulator processor.

proved through the increase in the SNR provided at the CRI output relative to the CRI input in the presence of wide-band interference. This increase depends upon the CRI loop gain, α , (Fig. 3) and equals $(1 + \alpha)/(1 - \alpha)$, [17]. With α selected to equal 0.85, a 10.9-dB improvement in SNR is obtained. Gain variations in the loop amplifiers, and ripple in the pass band in addition to the expected rate of change of the multipath profile play major roles in limiting the maximum nominal design value of the loop gain.

The SNR gain provided by the CRI is strongly dependent upon any residual carrier phase shift around the loop, such as caused by oscillator instability, SAW delay line length variations in manufacture, temperature effects, and Doppler effects. Fig. 6 shows the decrease in SNR improvement as a function of loop phase error assuming no loop bandwidth limitations. To maintain adequate control of the loop

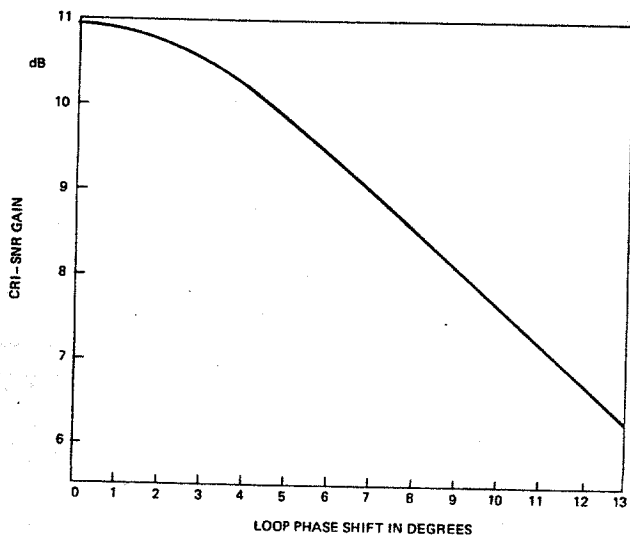


Fig. 6. SNR gain of CRI versus loop phase shift.

phase shift as a function of ambient temperature variations, (0°C to 55°C), the SAW delay line used in the CRI is placed in an oven. Under these conditions, the aggregate loop phase error (excluding Doppler) that can be reasonably expected is approximately $\pm 3^\circ$, maximum, leading to a decrease in SNR improvement of about 0.5 dB.

The SNR gain provided by the CRI is also dependent upon its loop bandwidth. Fig. 7 shows the CRI SNR gain plotted versus the loop bandwidth W_L normalized to the chip rate R_c assuming a sharp cutoff loop filter characteristic. Zero

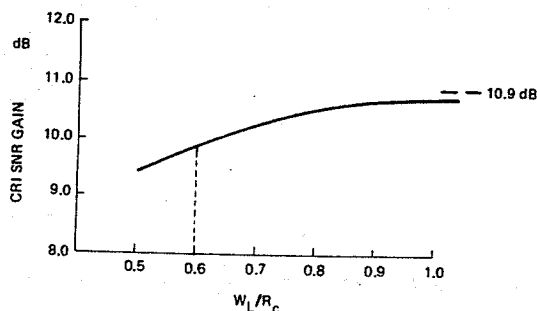


Fig. 7. CRI SNR improvement.

loop phase shift is further assumed. Practical bandwidth constraints limit operation to $W_L/R_c = 0.6$, resulting in an expected decrease of the SNR improvement of about 1.0 dB relative to the 10.9-dB theoretical value.

3) *Multipath Accumulation and Data Demodulation*: The multipath accumulation processor comprises the CRI, data demodulator, and integrate and dump circuit preceding the data decision circuit. The CRI builds up a replica of the multipath channel in amplitude and phase and is used as a coherent reference for data demodulation. The data demodulator demodulates (multiplies) this reference with the output signal from the MF. The MSK spread-spectrum signal enables the MF to resolve individual multipath signal components separated by approximately 1 chip, or about 78 ns from each other. The resulting weighted multipath components are summed in the integrate and dump circuit. The multiplication and integration approximate an optimum correlator to the multipath distorted input signal. This processing provides improved performance in a fading environment [5] for multipath spreads up to 6 μ s at the 100-kSPS rate, or 1.6 μ s at the 400-kSPS rate.

Two bits are output from the decision circuit to the microprocessor at each decision time: a sense bit and a quality bit. The sense bit is also fed back to the phase inverter (multiplier) in the decision directed CRI. The inverter output provides a data-free pulsed signal to the CRI. The quality bit is a measure of the symbol magnitude. It is used if the soft decision sequential decoding mode is selected. The noise estimator metric is used to set the threshold for the quality bit [18].

4) *Processing Gain and Anti-Jam (AJ) Margin*: The processing gain of the matched filter, determined by the time-bandwidth product of the waveform, provides protection against interference and jamming [19], [20]. In the presence of full band average power limited white Gaussian noise interference over the IF bandwidth, the PG is equal to the number of spread-spectrum chips processed in the matched filter; viz. $R_c T$, where R_c is the chip rate of 12.8 MCPS and T is the symbol duration. In the CRC modes, the PG is as shown in column (2) of Table 3.

Table 3 Matched Filter Processing Gain and Anti-Jam Margin (CRC)

(1)	(2)	(3)	(4)
Transmission Rate (kSPS)	PG (dB) Full-Band Interference	PG (dB) Near-Zero Bandwidth Interference	AJ Margin (dB)
100	21	19	9.4
400	15	13	3.4

For partial band interference, the PG is reduced by up to about 2 dB¹ as the interference bandwidth approaches zero. This more conservative measure of PG is shown in Table 3 column (3). The AJM is that part of the (near-zero bandwidth) PG which is in excess of the required symbol energy to noise density E_b/N_0 (9.6 dB), corresponding to the required BER (10^{-5}) [22]. The resulting AJM is listed in Table 3 column (4).

¹ $10 \log(\pi^2/16) = 2.1$ dB is the minimum-noise bandwidth factor for MSK modulation [21].

Table 4 Symbol FEC Gain

Code Rate	Symbol FEC Gain (dB)
7/8 S (soft decision)	4.6
3/4 H (hard decision)	4.6
3/4 S	6.6
1/2 H	7.5
1/2 S	9.5

Table 4 shows the effective symbol FEC gain and, hence, the increase in AJM expected versus code rate compared to the uncoded CRC mode for either symbol rate [18]. With FEC the value of the symbol SNR required to achieve the specified BER equals the uncoded value of E_b/N_0 divided by the effective symbol FEC gain. Thus the net PG available with 1/2 rate coding and hard decision is 19 + 7.5 or 26.5 dB at 100 kSPS providing an AJM of 16.9 dB.

D. Frequency Agility

The LPR has the capability of changing frequencies on a packet-by-packet basis as determined by the upper layer protocols. This can provide additional processing gain against certain types of interference including system self-interference and jamming. This feature provides frequency diversity and additional antimultipath processing capability since the normal packet retransmission can occur at a different frequency.

E. Tracking

Once bit synchronization is obtained, an open-loop time base is set at the nominal incoming data rate. The maximum number of symbols expected by the LPR in a processed packet equals 6556. At a symbol duration of 10 μ s, the maximum length packet lasts for 65.56 ms. Cost-performance tradeoffs resulted in transmitter and receiver clock accuracies of $\pm 1/2$ ppm. For radio pairs experiencing a relative Doppler velocity of ± 2000 ft/s the maximum timing error, or drift, expected equals ± 197 ns. This causes a negligible reduction of 3 percent of the 6- μ s integration window used in the multipath accumulator.

F. Time Synchronization

To allow packet radio networks to acquire and maintain time synchronization, time transfer between packet radios is necessary. This is accomplished in the LPR by time stamping incoming packets at the radio receiver and allowing the higher layer protocols the option of transmitting a time tagged packet. Both the time tagging and the stamping functions are performed relative to the frame sync epoch. The time tag value is appended to the end of the data portion of the packet before the final CRC. The minimum length of a time tagged packet is bounded by the time needed to obtain the time tag from the real time clock, send it to the CRC check circuit, get the CRC check, send both the time tag and the CRC check to the convolutional encoder, and obtain the encoded words from the convolutional encoder. The minimum length is 600 μ s.

G. Metrics

Upper layer protocols track radio link conditions through signal metrics provided by the LPR receiver. The available

metrics are AGC control voltage, noise estimate, signal plus noise estimate, indication of multipath spread, and, when FEC is employed, a symbol error rate estimate. The smoothed AGC control voltage provides an estimate of in-band power (including signal, noise, and interference) during the packet. The noise estimate, obtained from the noise estimator after low-pass filtering the envelope detected CRI output, is used to set all the threshold levels. The signal plus noise estimate provides an indication of signal strength and is obtained by peak detecting the output of the CRI. Multipath spreads greater than 1.6 μ s are detected and, if present, a multipath indicator is set. The sequential decoder outputs an estimate of the number of errors corrected. This is used as a symbol error rate measurement.

H. LPR Processor

The processor contains the hardware and software necessary to implement the link and network level protocol interpreters in the packet radio system and to interface the

- transmitter-receiver
- high-speed data interface
- low-speed data interface.

The processor is partitioned into four sections as shown in Fig. 8. The CPU section contains the 8086 CPU and peripherals (which include the low-speed serial data port, timers, and programmable interrupt controllers) to fulfill protocol functions, initialization, and debug/repair activities. The speed of the 8086 processor available for protocol processing is calculated to be in excess of 0.3 MIPS. The memory section contains 64K bytes of system ROM and 96K bytes of system RAM. The transmitter-receiver buffer section contains dual 8089 I/O processors, an A/D converter, and other peripherals that include the radio transmitter buffer, convolutional encoder/sequential decoder, CRC encoder/decoder, real-time clock/PN code generator, radio status/control registers, and subsystem RAM and ROM. The A/D converter digitizes the AGC, signal plus noise and noise metrics. The HDLC section contains the Physical and Data Link Layers for the serial high-speed wire data port.

V. LPR EXPECTED AND MEASURED PERFORMANCE COMPARISON

Several development LPRs were built and their acquisition and data demodulation performance were measured. Link performance specifications require the LPR to be able to acquire and demodulate packets under the following conditions:

- 10-km link range,
- 5-W transmitter power,
- ≥ 0.95 probability of acquisition,
- $\leq 10^{-6}$ probability of false acquisition,
- $\leq 10^{-5}$ BER.

Table 5 shows the RF link power budget at a 10-km range.

Table 5 Available Signal and Thermal Noise Power

Transmitted signal strength	37 dBm
Antenna gains (transmit/receive)	12 dB
Path loss at 10 km	-148 dB
Received signal strength (at antenna port)	-99 dBm

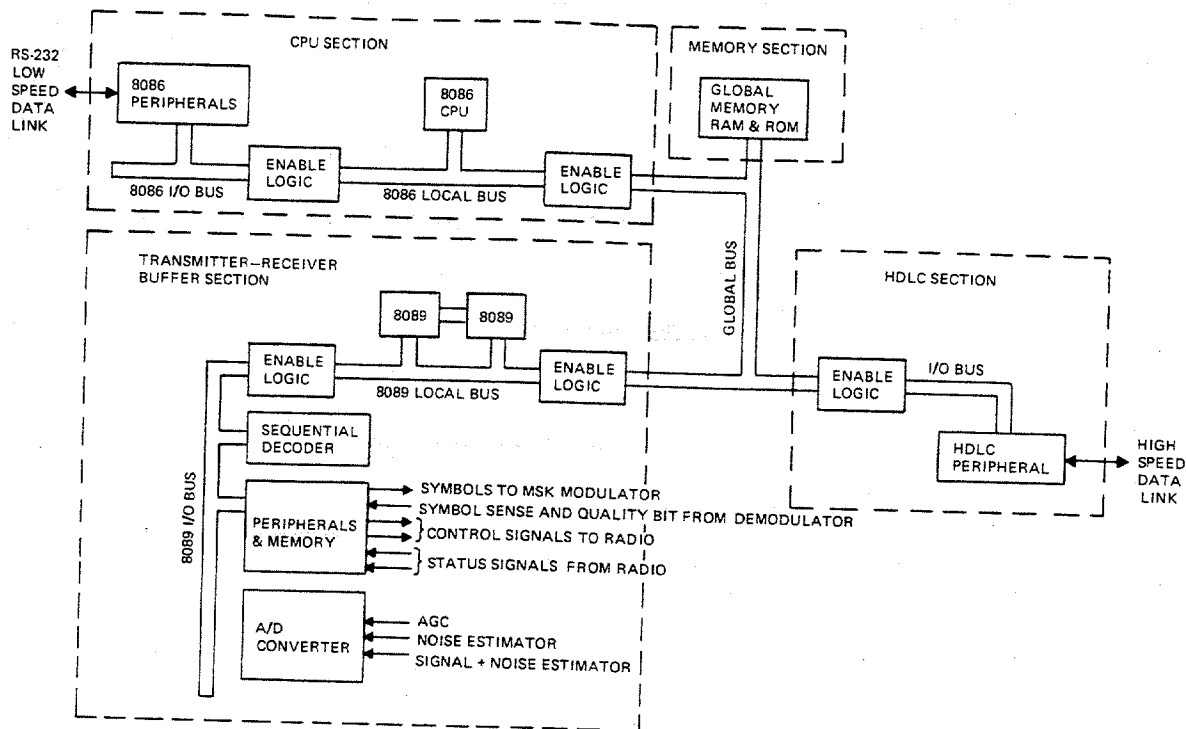


Fig. 8. LPR microprocessor system.

The calculated path loss was derived from the Longley-Rice model, as required by the specification, for antennas 1.5 m above the ground, 15- to 45-m rolling hills, and a transmitted frequency of 1.775 GHz.

Table 6 presents average measured data (measurement accuracy ± 1 dB), taken on several developmental models of the radio. The data show the average sensitivity signal

Table 6 LPR Measured Performance

Mode	Received Signal Power (dBm)	Margin (dB) (Relative to -99 dBm)
Synchronization	-109	10
1B 50 kbits/s (1/2 Rate H)	-107	8
1C 75 kbits/s (3/4 Rate H)	-108	9
1D 87.5 kbits/s (7/8 Rate)	-106	7
1A 100 kbits/s (CRC)	-104	5
2B 200 kbits/s (1/2 Rate H)	-99	0
2C 300 kbits/s (3/4 Rate H)	-100	1
2D 350 kbits/s (7/8 Rate)	-99	0
2A 400 kbits/s (CRC)	-96	-3

performance for acquisition and data demodulation at various data rates, and the margin relative to the calculated available power (-99 dBm).

The data show that the required acquisition and data performance were obtained at the 10-km range at all code rates except the 400-kbit/s CRC mode. The required performance in the 400-kbit/s CRC mode is expected to be obtained at a power level of 6 dB above the level achieved in the 100-kSPS mode, or -98 dBm. The additional 2 dB of power (-96 dBm) required in this mode is a result of nonlinear effects in the envelope detector and threshold processors.

The data also show that the expected coding gain for the 7/8 and 3/4 FEC rates were approximately obtained for both symbol rates. The coding gain for the 1/2 rate FEC fell short of the expected amount by almost 4 dB for both symbol rates. This degradation is primarily due to nonlinear transfer characteristics of the data demodulator at low levels.

Three LPR development models were deployed in a small, on-the-air, packet radio network, depicted in Fig. 9. The LPR was operated with the Survivable Radio Protocol "SURAP 1.0" [1]. The functionality of the hardware under the control of the software was verified. Alternate routing between LPR

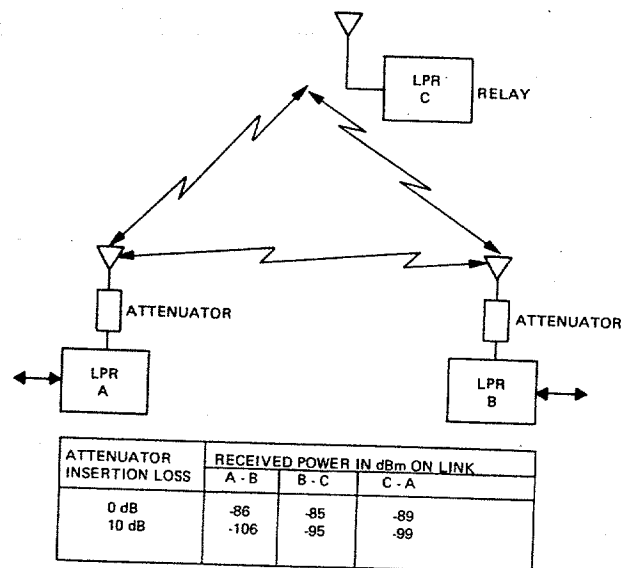


Fig. 9. LPR on-the-air network.

Table 7 Specification Compliance

	Specification	Measurement	Spec Met (x)
Antenna gain	5 dB	6 dB	
Transmitter bandwidth flatness	±2 dB	±0.8	x
Transmitter spurious frequencies	50 dB down	60 dB	x
Transmitter harmonic frequencies	50 dB down	68 dB	x
Receiver image rejection	60 dB down	70 dB	x
Receiver bandwidth flatness	±2 dB	±0.6 dB	x
Interference rejection in band	10 dB above signal	met for some test conditions	
Interference rejection out band at ±15 MHz	60 dB above signal	met at ±20 MHz	
Local oscillator rejection	60 dB down	70 dB	x
Transmitter power	5-W minimum	5.8 W	x
Incidental AM	10 percent	6 percent	x
Noise figure	8 dB	7 dB	x
Dynamic range	80 dB (to -20 dBm)	85 dB	x
Frequency stability	1/2 ppm	1/2 ppm	x
AGC settling time	20 μs	15 μs	x
False alarm rate (fa)	8 fa/s	8 fa/s	x
Probability of detection ≥ 0.95	-99 dBm	-107 dBm	x
Bit error rate ≤ 10 ⁻⁵ (100-kbit/s CRC mode)	-99 dBm	-104 dBm	x

A and LPR B, via LPR C was demonstrated by inserting sufficient attenuation in the A and B LPR antenna coaxial cables to break the A-B link, causing the packet to be relayed over link A-C and C-B.

Table 7 shows specification compliance, with two minor short falls.

VI. CONCLUSIONS

The LPR has been shown to be capable of supporting the development and evaluation of advanced networking concepts, techniques, and protocols. This new version of a packet radio provides the flexibility to support experimentation, at reduced volume, weight, and cost in test beds containing a large number of widely dispersed and mobile nodes over unpredictable channels.

Laboratory measurements are continuing and improvements are being implemented in the development models as the LPR is transitioning into preliminary production. Further field measurements and experimentation on the link and network level are planned.

While the LPR was optimized as a tool for network research, the design is amenable to tailoring to specific applications. The modularity of the LPR facilitates modification to other applications, which may, for example, require different data or spread-spectrum chip rates, fast frequency hopping, frequency division multiple access, or operation in another RF band.

ACKNOWLEDGMENT

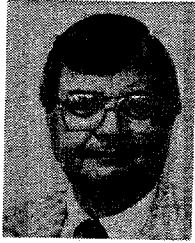
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